CLAIMS

What is claimed:

1. A method of erasing one or more non-volatile memory ("NVM") cells comprising.

applying to the one or more NVM cells an erase pulse having a substantially non-constant voltage profile

2 The method according to claim 1, wherein the voltage profile of the erase pulse is predefined.

3 The method according to claim 2, wherein the erase pulse has a voltage profile selected from the group consisting of ramp-like, trapezoidal, exponential-growth-like, asymptote-like and stepped

4 The method according to claim 3, wherein the erase pulse is applied to each sub-set of a set of NVM cells in a staggered sequence.

5 The method according to claim 1, wherein the voltage profile of the erase pulse is dynamically adjusted based on feedback.

6 The method according to claim 5, wherein the feedback comes from a sensor selected from the group consisting of a current sensor, a voltage sensor, a current derivative sensor, and a voltage derivative sensor.

7. The method according to claim 6, wherein the voltage of the erase pulse is adjusted in an inverse relation to current measure by the current sensor

8. The method according to claim 6, wherein the voltage of the erase pulse is adjusted at a rate correlated to a signal produced by the current derivative sensor

9 A circuit for erasing one or non-volatile memory ("NVM") cells comprising an erase pulse source to produce an erase pulse having a substantially non-constant voltage profile

10 The circuit according to claim 9, wherein said erase pulse source comprises a charge-pump.

11 The circuit according to claim 10, wherein the erase pulse source is adapted to produce an erase pulse having a voltage profile selected from the group consisting of ramp-like, trapezoidal, exponential-growth-like, asymptote-like and stepped.

12. The circuit according to claim 9, further comprising a cell select circuit adapted to select to which cells of a set of NVM cells the erase pulse is applied

13 The circuit according to claim 12, wherein said cell select circuit is adapted to apply the erase pulse to each sub-set of the set of NVM cells in a staggered sequence

14 The circuit according to claim 9, further comprising a sensor to sense a characteristic of the erase pulse as it is being applied to the one or more NVM cells

15. The circuit according to claim 14, wherein the sensor is selected from the group consisting of a current sensor, a voltage sensor, a current derivative sensor, and a voltage derivative sensor

16. The circuit according to claim 15, further comprising a controller to cause the erase pulse source to adjust the voltage profile of the erase pulse based on a signal from said sensor.

17 The circuit according to claim 16, wherein said controller causes the voltage of the erase pulse to be adjusted in an inverse relation to current measure by the current sensor.

18 The circuit according to claim 16, wherein said controller causes the voltage of the erase pulse to be adjusted at a rate correlated to a signal produced by the current derivative sensor.

19. A system for erasing one or non-volatile memory ("NVM") cells comprising:

A NVM array, and

an erase pulse source to produce an erase pulse having a substantially non-constant voltage profile